An Energy-Efficient Comparator with Dynamic Floating Inverter Pre-Amplifier

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Abstract

This paper presents an energy-efficient comparator with a novel dynamic pre-amplifier (pre-amp). By using an inverter-based input pair powered by a floating reservoir capacitor, the pre-amp realizes both current reuse and dynamic bias, thereby significantly boosting g_m/I_D and reducing noise. Moreover, it greatly reduces the influence of the input common-mode (CM) voltage on the comparator performance, including noise, offset, and delay. A prototype comparator in 180nm achieves 46uV input-referred noise while consuming only 1pJ per comparison under 1.2V supply. This represents >7x energy efficiency boost compared to a Strong-Arm (SA) latch. It achieves the highest reported energy efficiency to authors' best knowledge.

Introduction

Comparator bridges the analog and digital world [1]–[5]. A low-power low-noise comparator is critical for many circuits (e.g., SAR ADC). A comparator consists of a pre-amp followed by a latch. Unlike static comparators, dynamic comparators (e.g., SA latch) replace static pre-amps by dynamic integrators, which remove static current and reduce power. However, a conventional dynamic integrator based pre-amp has several limitations: 1) no current reuse is achieved; 2) it fully discharges load capacitors, even though only the initial discharging contributes to noise reduction; 3) due to limited integration time bounded by the output CM voltage drop, the effective pre-amp gain is low, leading to increased input referred noise and offset; 4) the comparator performance (e.g., noise, offset, and speed) depends strongly on the input CM voltage due to the lack of a tail current source.

There are emerging efforts to design better dynamic comparators. [1] realizes current reuse via bi-directional integration, but its extra circuit cost limits the energy efficiency boost to 1.5x compared to an SA latch. [2] uses dynamic bias to increase g_m/I_D and prevent fully discharging the load. It achieves 3.3x energy efficiency boost, but it does not realize current reuse. In addition to relatively limited efficiency boost, neither [1] nor [2] addresses the input CM dependence problem.

This paper presents an energy-efficient dynamic comparator with a floating inverter amplifier (FIA) based pre-amp. Its inverter-based input stage naturally realizes 2-time current reuse. Moreover, the inverter stage is powered by a floating reservoir capacitor that forms an isolated power domain, making the pre-amp operation independent from the input CM voltage. Thus, the comparator performance becomes much less sensitive to the input CM variation. The pre-amp output CM is also kept constant during the amplification process. Hence, the pre-amp gain is no longer limited by the output CM drop and can be much bigger. Furthermore, the reservoir capacitor provides dynamic source degeneration that increases g_m/I_D and prevents full discharge of the load capacitor. Overall, the proposed comparator achieves >7x energy efficiency improvement compared to the SA latch and much stronger common-mode rejection.

Proposed Comparator with FIA

As shown in Fig. 1, the proposed comparator consists of an FIA stage and a standard SA latch. During the reset phase (clk=0), the reservoir capacitor C_{RES} is pre-charged to V_{DD}/G_{ND}, and the pre-amp output V_A is reset to $V_{CM}=V_{DD}/2$. When the comparison starts, the FIA performs the dynamic integration, and its output V_A is sent to the SA latch to make the decision ($\Phi_{amp}=1$). Once the SA latch resolves, the FIA is disabled to prevent further discharge of C_{RES} to save energy ($\Phi_{amp}=0$). With the sufficient gain (>20) provided by the FIA (see Fig. 1), the noise contribution from the SA latch is negligible, and thus, a minimum size SA latch is used for power saving.

Fig. 2 depicts the model of the CMOS dynamic integration by the FIA stage. Two equivalent $2C_{RES}$ serve as the degeneration capacitors for NMOS and PMOS input pairs. During amplification, the input signal is dynamically-biased integrated [2] by the CMOS input pair. The simulated g_m/I_D during integration is shown in Fig. 2. Unlike the SA latch whose (V_{GS}–V_{TH}) of the input pair stays constant, resulting in a fixed g_m/I_D, (V_{GS}–V_{TH}) of both FIA NMOS and PMOS input pairs are decreasing during FIA operation, thus boosting the average g_m/I_D by >3x, leading to significant improvement in energy efficiency. Note that with larger input CM voltage, this efficiency boost will be even bigger due to the constantly low g_m/I_D of the SA latch under large V_{GS}. Furthermore, as shown in Fig. 1, the integration nodes V_{A+}/V_{A-} are only partially charged/discharged, which also saves considerable energy.

Fig. 3 shows the FIA behavior with different input CM voltages. As it is powered by a floating reservoir capacitor, the FIA pre-amp works in its own isolated voltage domain. Since the input/output current from C_{RES} must be equal, we can derive that $I_{INT+} = I_{INT-}$, leading to a constant output CM voltage [6]. Thanks to the floating nature of FIA, not only its output CM voltage, but also its gain and speed are input CM insensitive. As shown in Fig. 3, with input CM voltage varying from 0.4V to 0.8V, the output CM voltage remains constant. The variation in the settled FIA gain is also small (<10%). The simulated transient behaviors of the FIA are shown in Fig. 4. The input CM voltage variation only causes a voltage level shift for V_{RES+}/V_{RES-}, which automatically balances the NMOS and PMOS overdrive voltages. As a result, the overall FIA operation is unaffected. The simulated CLK-Q delay vs. input CM voltage variation is shown in Fig. 5. With a low input CM, the delay of the SA latch increases significantly. By contrast, the proposed comparator has a much smaller variation, which again attests its insensitivity to the input CM variation.

Measurement Results

As shown in Fig. 6, the prototype is fabricated in 180nm CMOS along with a standard SA latch for comparison, whose NMOS input pair size is 2x of the ones in the FIA stage so that they share the same initial g_m. The measured cumulative distribution functions (CDFs) for the two comparators are shown in Fig. 7. The extracted rms input referred noise voltages are 62uV for the SA latch and 46uV for the proposed comparator with FIA. Fig. 8 shows the measured comparator noise and offset variation vs. the input CM variation. During the offset variation measurement, both comparators are

calibrated at 0.6V input CM voltage. As expected, the proposed comparator exhibits much less variation and shows consistently lower noise.

Table I summarizes the performance for different comparators. The figure-of-merit (FoM) is defined as the product of energy and noise power to reflect the energy efficiency (smaller is better). Overall, the proposed comparator with FIA achieves >7x improvement over the classic SA latch and 2.7x improvement over the 2nd best [2]. To authors' best knowledge, it is the most energy efficient comparator reported to date. It also provides much stronger CM rejection.

References

[1] M. Liu, et al, ISSCC, 2015.
[2] H. S. Bindra, et al, JSSC, 2017.
[3] M. Miyahara, et al, ASSCC, 2009.
[4] M. van Elzakker, et al, JSSC, 2010.
[5] D. Schinkel, et al, ISSCC, 2007.
[6] M. S. Akter, et al, VLSI, 2017.

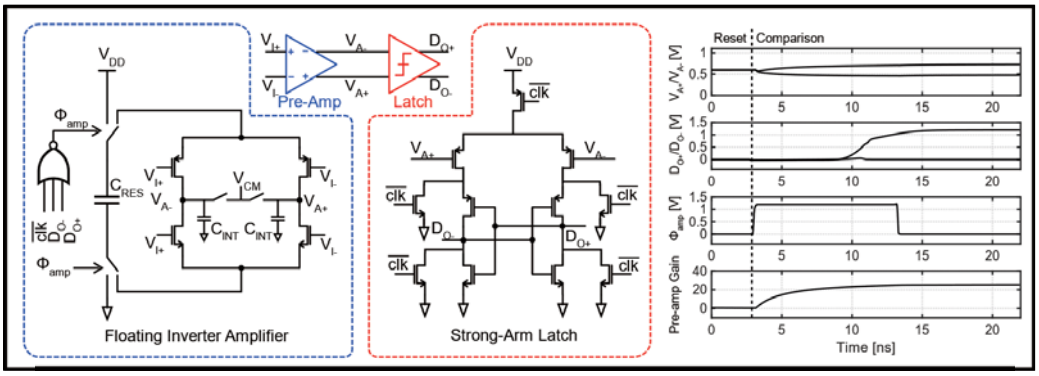

Fig. 1 Schematic and operation of the proposed comparator with FIA based pre-amp.

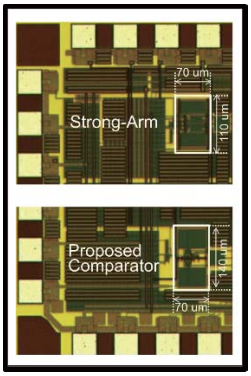

Fig. 6 Die micrograph.

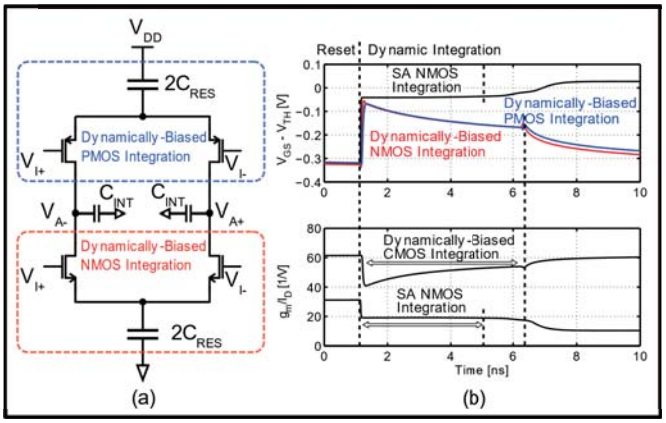

Fig. 2 (a) Equivalent model of the dynamically-biased CMOS integration. (b) Simulated V_{GS}–V_{TH} and g_m/I_D with 1.2V supply and 0.6V input CM voltage.

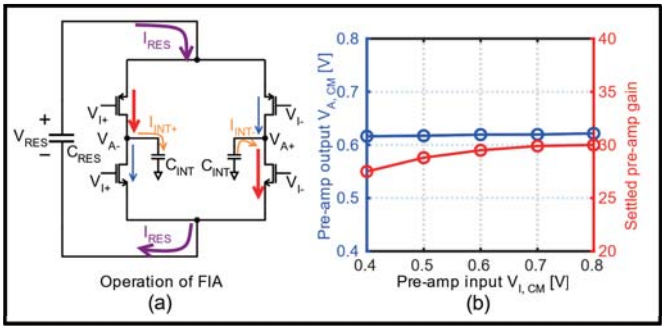

Fig. 3 (a) Illustration of the FIA CM behavior. (b) Simulated pre-amp output CM voltage and gain as a function of the input CM voltage.

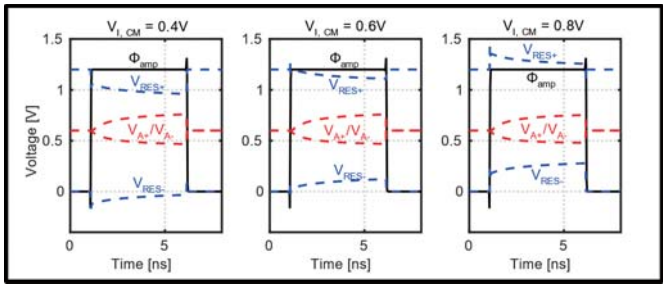

Fig. 4 FIA behavior with input CM voltage of 0.4V, 0.6V, and 0.8V.

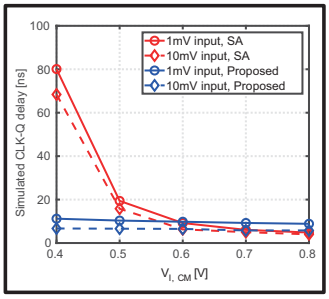

Fig. 5 Simulated CLK-Q delay vs. input CM voltage.

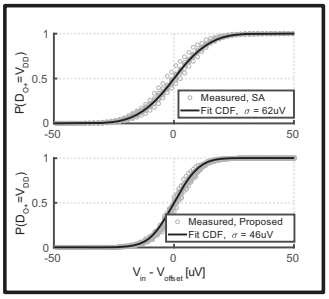

Fig. 7 Measured CDF with 1.2V supply and 0.6V input CM voltage.

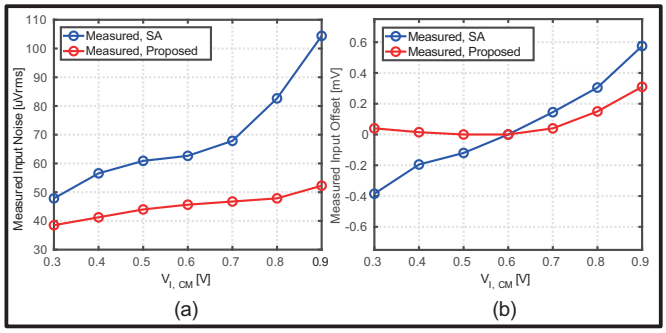

Fig. 8 (a) Measured input referred noise vs. input CM voltage. (b) Measured input referred offset variation vs. input CM voltage, calibrated at 0.6V input CM voltage.

	This Work		[2]		[5]
Featured Architecture	**Proposed FIA+SA**	Standard SA	Dynamic Bias	Double-Tail [4]	Double-Tail
Process [nm]	**180**	180	65	65	90
Supply [V]	**1.2**	1.2	1.2	1.2	1.2
Noise [uV]	**46**	62	400	450	1500
Energy [pJ]	**0.98**	4.1	0.034	0.088	0.113
FoM* [nJ·uV²]	**2.07**	15.8	5.44	17.8	254
Insensitive to Input CM voltage	**Yes**	No	No	No	No

*$FoM = Energy \cdot (Noise\ Power)$

Table I. Performance summary and comparison with latest dynamic comparators.